

REMARKS

In the above-identified Office Action, the Examiner objected to claim 37, and rejected claims 1-26 and 28-39 under 35 U.S.C. §103(a). These objections and rejections are fully traversed below.

Claims 1, 9, 17, 26 and 37 have been amended to further clarify the subject matter regarded as the invention. Claims 1-26 and 28-39 remain pending in this application.

Reconsideration of the application is respectfully requested based on the amendments and the following remarks.

CLAIM OBJECTIONS

In the Office Action, claim 37 was objected to due to a formatting informality. Claim 37 has been represented herein with appropriate formatting. Accordingly, it is respectfully requested that the Examiner withdraw the objection to claim 37.

REJECTION OF CLAIMS 1-26 AND 28-39 UNDER 35 U.S.C. §103

In the Office Action, the Examiner rejected claim 1-8 under 35 U.S.C. §103(a) as being unpatentable over Bartley (U.S. Patent No. 6,219,796) in view of Fletcher et al. (U.S. Patent No. 6,611,920) and Lin (U.S. Patent No. 5,787,297); rejected claims 9-16 over Bartley in view of Fletcher and Matter et al. (U.S. Patent No. 5,392,437); rejected claim 17-25 over Matter et al. in view of Bartley, Fletcher and Sproch et al. (U.S. Patent No. 6,247,134); rejected claims 26 and 28-36 over Bartley in view of Fletcher and Sproch et al.; rejected claim 37 over Matter in view of Bartley, Fletcher and Sproch et al.; and rejected claim 39 over Bartley, Fletcher, Lin and Simonovich (U.S. Patent 6,308,241). These rejections are fully traversed below.

The present invention pertains to methods and systems for saving power in pipelined processors. Specifically, claim 1 of the present invention requires the controlling of the supply of current to each of a plurality of stages of a functional unit after evaluating instructions and producing activity indicators, which facilitate the control of the supply of current. The method of claim 1 allows for efficient evaluation of operation type of each instruction so that power supplied to each stage of a functional unit can be individually controlled.

Among other things, claim 1 recites:

evaluating instructions to be executed to determine the operation type of each of said instructions, the instructions to be

executed depending on the operation type by said plurality of stages of said functional unit, where said stages of said functional unit are arranged in series;

producing activity indicators based upon the operation types of said instructions;

Bartley pertains to optimizing a computer program to provide better power management for microprocessors. Bartley operates to optimize computer code to insert “power-down” instructions for a functional unit when such is not needed. The power-related instructions are added manually by a programmer or by a compiler or assembler. See col. 7, lines 31-38. Here, the computer code is being altered. Hence, Bartley does not produce activity indicators as recited in claim 1. Furthermore, claim 1 pertains to instructions that are executed by a series arrangement of stages of a functional unit. Bartley also does not teach or suggest use of a multi-stage functional unit or individually controlling stages of a multi-stage functional unit. In addition, Bartley fails to teach or suggest controlling the supply of current immediately after evaluating instructions and producing activity indicators, which are used to control the supply of current to respective stages of a functional unit.

Fletcher pertains to a power control system in which a functional unit block can have stages that are separately powered. Presumably, powering of the stages is based on a valid indicator signal that is received by the functional unit block when valid data is input. Even so, in contrast to claim 1, Fletcher fails to provide any teaching or suggestion towards evaluating instructions to determine operation type and then producing activity indicators based upon the operation types of the instructions. Therefore, Fletcher et al. fails to teach or suggest the controlling of the supply of current to each of a plurality of stages of a functional unit immediately after evaluating instructions and producing activity indicators.

Lin describes a microelectronic device that can turn on and off its functional units under program control. Lin, like Bartley, fails to teach or suggest controlling stages of a multi-stage functional unit.

Moreover, there is no adequate motivation of record that one lead one of ordinary skill in the art to combine Bartley with either Fletcher or Lin. Bartley pertains to program optimization. Neither Fletcher nor Lin pertains to program optimization. Also, the optimization of the computer code in Bartley is, at best, used to control an entire functional unit. Thus, there is no suggestion on how such computer code would be used in the case of controlling separate stages of a multi-stage functional unit. Furthermore, there is no suggestion on how the optimized

computer code in Bartley would be used to produce valid indicator signals required by Fletcher. Still further, the program optimization in Bartley is not performed immediately before execution by a multi-stage functional unit. Hence, it is submitted that the combination of Bartley with either Fletcher or Lin is improper.

Accordingly, it is submitted that Bartley, Fletcher et al. and Lin, alone or in any combination, do not teach or suggest the features of claim 1.

Independent claim 9 and dependent claim 39 of the present invention pertain to methods that require receiving instructions at an instruction evaluation unit from an instruction register where the instruction evaluation unit evaluates the operation type of the instructions. The instruction register temporarily stores instructions before they are executed. As recited in claims 9 and 39, the instructions are evaluated for their operation type shortly before being executed. Depending on the operation types, the instructions can be executed by the plurality of stages of the functional unit, where the stages are arranged in series. In contrast, neither Bartley nor Fletcher et al. teach or suggest receiving instructions at an instruction evaluation unit from an instruction register where the instruction evaluation unit evaluates the operation type of the instructions. Matter et al. discloses an instruction cache which may, at best, correspond to an instruction register of claims 9 and 39; however, there is no teaching or suggestion for an instruction evaluation unit that receives instructions from the instruction register for evaluation. Therefore, it is submitted that Bartley, Fletcher et al. and Matter et al., alone or in any combination, do not teach or suggest the features of claims 9 and 39.

Independent claims 17 and 37 pertain to a microprocessor and system where an instruction evaluation unit is connected to an instruction register where the instruction evaluation unit evaluates the next instruction to produce activity indicators. Furthermore, claims 17 and 37 recited that a stage activation controller is connected to the instruction evaluation unit, wherein the stage activation controller utilizes the activity indicators to activate or deactivate each stage of a multi-stage functional unit. In contrast, neither Bartley nor Fletcher et al. teach or suggest an instruction evaluation unit that is connected to an instruction register where the instruction evaluation unit evaluates the next instruction to produce activity indicators. Also, neither Bartley nor Fletcher et al. teach or suggest a stage activation controller that is connected to the instruction evaluation unit. Therefore, it is submitted that Bartley, Fletcher et al., Matter et al. and Sproch et al., alone or in any combination, do not teach or suggest the features of claims 17 and 37.

Independent claim 26 pertains to a microprocessor that includes an instruction evaluation unit and a stage activation controller. The instruction evaluation unit evaluates a next instruction to be executed and produces activity indicators. The stage activation controller utilizes the activity indicators to activate or deactivate each stage of a multi-stage functional unit. In contrast, neither Bartley nor Fletcher et al. teach or suggest an instruction evaluation unit a stage activation controller or an instruction evaluation unit as recited in claim 26. Therefore, it is submitted that Bartley, Fletcher et al. or Sproch et al., alone or in any combination, do not teach or suggest the features of claims 26.

Based on the foregoing, it is submitted that claims 1, 9, 17, 26 and 37 are patentably distinct from Bartley, Fletcher et al., Matter et al., Sproch et al. and/or Simonvich. In addition, it is submitted that dependent claims 2-8, 10-16, 18-25, 28-36, 38-39 are also patentably distinct from Bartley, Fletcher et al., Matter et al., Sproch et al. and/or Simonvich for at least the same reasons as those recited above for their corresponding independent claims. The additional limitations recited in the dependent claims are not further discussed, as the above-discussed limitations are believed to be sufficient to distinguish the claimed invention from the cited references. Thus, it is respectfully requested that the Examiner withdraw the rejection of claims 1-38 under 35 U.S.C § 103(a).

SUMMARY

It is submitted that the objection to claim 37 has been overcome. In addition, it is submitted that claims 1-26 and 28-39 are patentable distinct from any combination of the cited art relied on by the Examiner. Therefore, it is submitted that claims 1-26 and 28-39 are patentably distinct from the cited references. Reconsideration of the application and an early Notice of Allowance are earnestly solicited.

If there are any issues remaining which the Examiner believes could be resolved through either a Supplemental Response or an Examiner's Amendment, the Examiner is respectfully requested to contact the undersigned attorney at the telephone number listed below.

If any fees are due in connection with the filing of this Amendment, the Commissioner is authorized to deduct such fees from the undersigned's Deposit Account No. 50-0388 (Order No. APL1P203).

Respectfully submitted,
BEYER WEAVER & THOMAS, LLP



C. Douglass Thomas
Reg. No. 32,947

BEYER WEAVER & THOMAS, LLP
Telephone: (650) 961-8300